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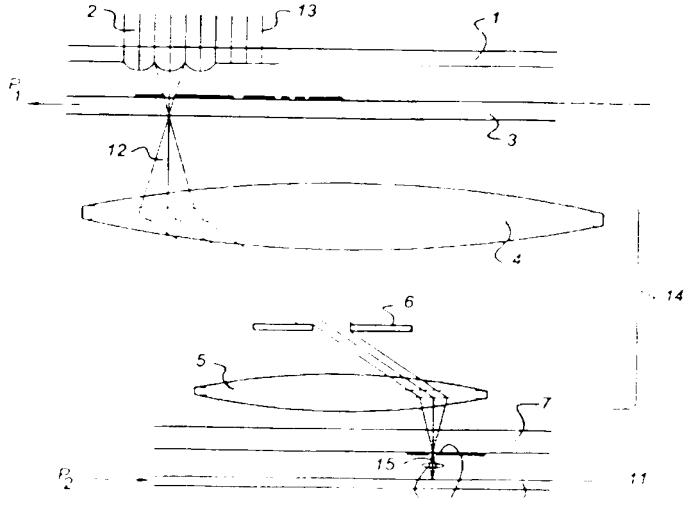
(54) Title: FIELD EMISSION PHOTOCATHODE ARRAY FOR LITHOGRAPHY SYSTEM AND LITHOGRAPHY SYSTEM PROVIDED WITH SUCH AN ARRAY



Field emission photocathode array for lithography system and lithography system provided with such an array.

Field of the invention

The invention relates to using an electron source for producing at least one electron beam directed towards and focussed on an object to be processed, the electron source comprising at least one field emitter.

The invention also relates to a lithography system provided with such a converter element.

Prior art

Converter elements for use in lithography systems, and designed to convert a light beam into a beam of charged particles are known from WO98/54620. The purpose of these converter elements is to provide a better resolution (0.1 μm or less) in such systems than was possible with prior art systems without such converters in which the resolution was entirely determined by the wavelength of the light beam used.

First of all a description of such a system as described in WO98/54620 is given. To that end, reference is made to Figure 1.

The background of the system described in WO98/54620 is as follows.

Imagine that there is provided a known deep-UV lithography tool (i.e., wavelength 193 nm or less) for the 0.13 μm generation with a "traditional" 4 x mask for obtaining the 0.1 μm generation. Then, at a wafer surface, each 0.4 μm "pixel" of a mask is focused to a spot of 0.13 μm. Since the distance between pixels at the wafer must be 0.1 μm, there is a mixing of information between neighbouring pixels because the spots of 0.13 μm overlap each other. If we could sharpen up this 0.13 μm spot, this machine would be ready for the 0.1 generation. The sharpening up, or enhancement of resolution, cannot be done after the mixing of information has occurred.

According to one embodiment described in WO98/54620 only one pixel of the mask is illuminated. Then there is only an isolated spot of 0.13 μm at an imaginary wafer plane. At the location of the spot in the imaginary wafer plane a converter element, for example in the form of a photocathode of size 0.1 μm, or a photocathode with a metallic aperture of diameter of 0.1 μm on top, is positioned. Such a photocathode provides an electron source that may have a diameter of 0.1 μm. The photocathode that

is obtained in this way is imaged with magnification factor 1 onto the wafer in a real wafer plane spaced from the photocathode. This can be done either with acceleration inside a magnetic field or with a small accelerating electrostatic lens. The next step is to move the mask, e.g., 0.4 μm in order to illuminate an adjacent pixel on the mask while, at the same time, moving the wafer 0.4/4 = 0.1 μm in order to have the adjacent pixel on the wafer written. In such a way, the mask pattern is transferred to the wafer with the required resolution.

However, it would take a long time to write a whole wafer with this single beam. However, the principle is the same when many pixels are written simultaneously. Therefore, a multiple beamlet embodiment can also be used. In theory, the distance between separate beams at the wafer surface needs only to be as much as the point spread function. In practice, certainly when electrostatic focusing is used, the fabrication technology of the photocathode/lens array will determine the minimum distance. The number of beams is estimated to be in the order of 10^6-10^8.

Such a multiple beamlet embodiment shown in Figure 1. A light source (not shown) produces a light beam 13, preferably in deep UV. The light beam 13 impinges on a micro lens array 1 having lenses 2. The light beam 13 is as it were divided in beamlets 12, of which only one is shown for the sake of clarity. However, in practice there may as much as 10^6 - 10^8 beamlets 12. The lens 2 focuses the beamlet 12 on a mask 3 with spots of, e.g., 400 nm diameter. Each light beamlet 12 leaving the mask 3 passes a demagnifier 14, which is schematically indicated by lenses 4 and 5 and an aperture 6. However, other types of demagnifiers known from the prior art may be used instead. By the demagnifier 14 the beamlets 12 are focused on a converter plate 7 having converter elements 8 of which only one is indicated. If, as disclosed by WO98/54620, the converter plate 7 is constituted by a photocathode having a plurality of apertures a plurality of electron beamlets 15 (only 1 being shown in Figure 1) is generated. The electron beamlet 15 originates from the aperture and passes through focusing means, indicated schematically by a lens 9. Finally, the electron beamlet 15 impinges on the wafer 10 in wafer plane 11.

0.1 μm. Pixels could be arranged at random on the wafer 10. In an embodiment shown in Figure 2, the wafer pixels are arranged in lines and columns and the exposure direc-

tion SCAN differs from the direction of the lines of pixels.

The resolution is enhanced by sharpening up pixel by pixel, using a photocathode with very many apertures. This known technology is called "Multiple Aperture Pixel by Pixel Enhancement of Resolution" or "MAPPER" technology. It can be thought of as traditional projection lithography in which the mask information is split up and transferred to the wafer sequentially. It can also be thought of as multiple microcolumn lithography in which the electron sources are blanked by the mask.

WO98/54620 suggests that the photocathode could be replaced by an array of field emitters. However, by that time it was thought that this could only be achieved by providing for each field emitter individual control by light switches on which the light beamlets impinge. This is a complex arrangement.

Summary of the invention

It is an object of the invention to provide a field emitter photocathode array for a lithography system that can be produced relatively easily and can produce electron beams originating from a very small area.

To that end, the invention provides a use as defined at the outset, wherein the electron source comprises a semiconductor layer with at least one tip, and the use includes the steps of:

- receiving light by the semiconductor layer;
- exciting electrons to a conduction band by the light within said semiconductor layer by a photo-electric effect;
- accelerating the electrons in the conduction band towards the at least one tip and tunnelling them outside the at least one tip in order to generate electrons for said electron beam.

During their research carried out to find a suitable structure from a suitable material, the inventors found that they had to look for a material with the following properties:

- the material should exhibit a field emission effect;
- the material should be able to convert light beamlets with a wavelength of, 400 nm or less, e.g., 193 nm, into charged particles with a relatively high conversion factor;
- the material should allow to manufacture a converter plate with a plurality of charged particle sources of very small size, i.e., for instance 100 nm or less,

preferably 50 nm or less, in diameter, and far enough apart to prevent overlap of adjacent charged particle beams to prevent mixing of information;

- the charged particle sources should be capable of being switched on and off by switching on and off the light beamlets impinging upon the charged particle sources with a frequency of, e.g., 2 MHz or more;
- the charged particle sources should be very stable and capable of resisting relatively high pressures, e.g., pressures higher than 10^{-7} mbar.

It turned out that such a material of suitable structure had already been proposed for another field of technology, i.e., the field of image-tubes, a long time ago. The inventors found that a semiconductor field emission array for image-tubes as disclosed by Schroder e.a. in the beginning of the seventies in "The semiconductor field-emission photocathode", IEEE Transactions on Electron Devices, Vol. ED-21, No. 12, December 1974, could meet these requirements and, thus, advantageously be used in the recently developed MAPPER lithography concept, referred to above.

Moreover, it is a further object of the invention to provide a lithography system provided with such a field emitter photocathode array.

Therefore, the invention also relates to a lithography system comprising an electron source for receiving light and converting light in at least one electron beam directed towards and focussed on an object to be processed, electron source comprising at least one field emitter, wherein the electron source comprises a semiconductor layer with at least one tip, and the lithography system being arranged to:

- receive the light by said semiconductor layer;
- excite electrons to a conduction band by the light within the semiconductor layer by a photo-electric effect;
- accelerate the electrons in the conduction band towards at least one tip and tunnel them outside at least one tip in order to generate electrons for electron beam.

Advantageous embodiments of the invention are defined in depending claims.

Brief description of the drawings

Figure 1 shows schematically a lithography system according to the prior art in which the field emitter photocathode array can be used;

Figure 2 shows an example of a scanning direction of pixels on a wafer to be lithographed;

Figure 3 shows a Scanning Electron Microscope image of a p-type silicon wafer with an array of tips;

Figure 4 shows schematically the operation of a semiconductor field emission array as shown in Figure 3 in a MAPPER setup;

Figure 5 shows a band energy scheme of a semiconductor field emission array as shown in Figure 3;

Figure 6 shows the current on a logarithmic scale flowing from a tip of a semiconductor field emission array as shown in Figure 3, as function of the inverse voltage across the tip.

Figure 7 shows an embodiment of the semiconductor field emission array made of a very thin layer.

Figures 8a, 8b, 9a, and 9b show several energy band curves for an interface layer between a semiconductor layer and a supporting layer;

Figures 10a and 10b show holes in the semiconductor layer to prevent cross talk between adjacent electron sources.

Description of preferred embodiment

Figures 1 and 2 have been explained above.

In accordance with the invention the converter plate 7 comprises a semiconductor field emission array as shown in Figure 3. Figure 3 shows a plurality of tips on a p-doped silicon substrate. The image has been made by means of a Scanning Electron Microscope (SEM). The silicon wafer was sized 5 mm x 5 mm. 81 x 81 tips were etched on the wafer surface. The tips shown were spaced about 8 μm whereas their height was about 4 μm. Of course, these figures are only examples. To further enhance the resolution on the wafer 10 to be processed, it is envisaged that the tips may be located closer to one another than 8 μm.

The front surface from the tips, from which the electrons leave the silicon, have a diameter of preferably less than 100 nm, even more preferably less than 50 nm.

Figure 3 shows conically shaped tips. However, the invention is not limited to such a shape. The tips may have a rectangle or other shaped cross section, or be shaped like a sphere.

A structure a shown in Figure 3 has been disclosed by Schroder e.a. referred to above. It has the following characteristics:

- field emission is limited by the availability of electrons in the operating regime;
- electrons are excited from the valence band in the conduction band by photons from the impinging beamlets 12;
- tunnel probability approaches 1;
- due to field penetration in the tips the sources are less sensitive for pollution than metallic emitters.

Figure 4 shows the operation of the semiconductor field emission array 7 in more detail. The array 7 comprises a supporting substrate 17, e.g., made of Pyrex, but any other suitable material can be used. The supporting substrate must be made from a material that has a very low absorption factor for the wavelength of the light beamlets 12. For instance, when UV light is used the material may be quartz. On top of the supporting substrate 17 a semiconductor point array layer 16 is provided, preferably made of p-doped silicon. However, by applying another semiconductor material the bandgap between the valence band and the conduction band may be tuned to the wavelength of the light beamlets 12 used.

The structure shown in Figure 4 is used in the transmissive mode, i.e., light beamlet 12 impinges on the supporting substrate 17. The material used for the supporting substrate must be transparent to the wavelength of the light used. The photons from the light travel through the supporting substrate 17 and reach the semiconductor layer 16 where they will generate electrons, as will be further explained with reference to Figure 5 below.

The electrons leave the silicon layer 16 substantially at the front surface of the tips 19. An external (constant) electrical and magnetic field 18 accelerate the electrons and focus them on the wafer 10 to be processed. The electrical and magnetic fields are preferably directed in parallel from the silicon layer 16 towards the wafer 10 to be processed.

Although Figure 4 shows light beamlets 12 impinging on the converter plate 7 on the

Moreover, the generated electrons may be accelerated and focussed by other means, as is known to persons skilled in the art.

Figure 5 shows the energy bands of the silicon layer 16. The vertical axis shows the energy and the horizontal axis shows the position within the silicon layer 16. The most relevant energy bands are shown:

- E_c = energy of the conduction band;
- E_v = energy of the valence band;
- E_f = energy of the Fermi level, which is between E_c and E_v.

The vertical line at the right hand side of the energy bands corresponds to the boundary of the tip 19 at the interface with the external vacuum. The most right bevelled line corresponds to the external electrical field. Its inclination is determined by the strength of the external electrical field.

Since the conversion material is made from a semiconductor there are few electrons in the conduction band E_c. By illuminating the semiconductor with light a photoelectric effect occurs within the semiconductor material. A photon excites an electron from the valence band E_v to the conduction band E_c.

Figure 5 shows that the energy bands are curved at the outside surface of the tips 19. This is caused by the external electrical field that penetrates the semiconductor material. The curved energy bands cause electrons, indicated with "e", in the conduction band E_c to be accelerated towards the interface of tips 19 and the external vacuum. During their acceleration within the semiconductor material, these electrons may excite further electrons from the valence band to the conduction band. On the other hand, some of the electrons will fall back to the valence band. Including this latter effect, still an efficiency of 1 for the conversion of electrons per photon may be obtained. At the same time, holes, indicated with "h", left behind in the valence band E_v are accelerated in the opposite direction. When a high external electric field is applied there is a high change for electrons in the conduction band E_c to tunnel from the material towards the external vacuum.

The electrical current thus generated by the impinging photons is mainly determined by the availability of electrons in the conduction band E_c and less by the external electrical field strength.

Figure 6 shows the electrical current generated by the impinging photons on a logarithmic scale as a function of the voltage across the tips 19. The voltage is shown on an inverse scale, i.e., the voltage increases going from right to left.

Figure 6 shows that, starting at the right hand side of the curve, when the voltage

increases above a certain first threshold the log current starts to deviate from a straight line and smooths to a more or less constant level. When the voltage increases further above a second threshold the log current increases sharply and returns to the original straight line.

In the region where the log current is smoothed the actual log current strength depends on, for instance, temperature and the amount of light in the beamlets 12. Therefore, in this region the current strength can be controlled by the impinging light. This effect is discussed in detail in the article of Schroder e.a. referred to above.

Preferably, light is used having a wavelength of 400 nm or less, e.g., 193 nm.

The pressure within the system shown in Figure 1 may be higher than 10^{-7} mbar. Even with such a relatively high pressure, the converter element 7 is stable.

In Figure 7 an embodiment of the semiconductor emission array 7 is shown with a thickness of typically 100 nm or less. Typically the thickness of the semiconductor emission array 7 may be 20-30 μm, however, by making the semiconductor layer 7 so thin, electrons generated at the side that is illuminated by the beamlets 12 have either themselves a higher change of reaching the tips 19 or generate secondary electrons by collisions with semiconductor atoms that may reach the tips 19. Therefore, the embodiment of Figure 7 improves the efficiency of the converter element 7.

Figure 8a shows how the valence bands (lower curve) and conduction bands (upper curve) within a quartz substrate 17 and the semiconductor layer 16 will be as a function of location when these two layers are connected to one another. As shown, in an interface layer with a thickness of d1 the band pattern shows a pit. The pit causes electrons generated in this interface layer to have great difficulty in flowing to the tip side of the semiconductor layer 16, thus decreasing the efficiency of conversion.

The efficiency can be improved by depositing the quartz layer 17 on the semiconductor layer 16 very slowly in a controlled way. Then, the width of the interface layer will be decreased to d2 (d2 < d1). Such a smaller width d2 results in less electrons being trapped in the interface layer and, thus, more electrons being capable of reaching the tips 19 of the semiconductor layer 16.

Figure 9a shows the pit in the interface layer without such H ions being added. Figures 9a and 9b (as well as Figures 8a and 8b) are not on scale but they give a fair impression

of the effects concerned. The H^+ ions compensate the electron configuration in the interface layer. Instead of H^+ ions other atoms/ions may be used to provide this effect.

In the Mapper system of Figure 1, it is important that each light beamlet 12 triggers only one electron beam via one tip 19 and does not trigger any of its adjacent tips 19. This may be facilitated by removing material in the semiconductor layer 16 behind the tips 19. This may be done by making rectangular or other holes 20 in the semiconductor layer 16 surrounding the tips 19 as shown in Figures 10a and 10b. Figure 10a shows a cross section through such a semiconductor layer 16 whereas Figure 10b shows a top view.

In order to prevent spherical aberrations from adversely affecting the imaging from electron sources on the object 10, a diaphragm may be located behind each of the tips 19. These diaphragms decrease the aperture angle from the electron beams at the tips 19.

It is observed that the invention has been illustrated above with reference to its use in a multiple light beam lithography system as shown in Figure 1. However, the invention can also be used in other types of lithography systems. For instance, instead of modulating the beamlets 12 with mask 3, they may be modulated by modulating sources that produce them. Moreover, as a further alternative, the invention may be used in any single beam or multi-beam electron lithography system, e.g., an "electron beam direct write" system. Electron sources used in such systems should have the following features:

- very small source dimensions;
- high current per electron source, i.e., high brightness;
- high stability over time;
- large homogeneity between individual electron sources when a plurality of sources is used at the same time;
- a large bandwidth, i.e., the sources must be capable of being switched on and off with a high frequency.

All these requirements can be met by the semiconductor field emission array proposed here.

In other types of lithography systems (not shown), then, the semiconductor field emission array 7 may, e.g., be illuminated by a single light beam 13. Then, no mask 3 and demagnifier 14 are used. By illuminating the entire field emission array 7, all tips

19 will generate electrons simultaneously. By means of alignment deflectors, each electron beam can be accurately positioned through a small blanking aperture on the object 10 to be processed. Blanking electrodes may be used to turn the individual electron beams on and off at the vicinity of the object 10 in order to write a desired pattern on the object surface. An example of such a multi-beam direct write electron beam lithography system in which the semiconductor field emission array 7 could be used is described in: Dot matrix electron beam lithography, T.H. Newman, R.F.W. Pease and W. DeVore, J. Vac Sci. Technol. B1, 999 (1983).

Claims

1. Use of an electron source (7) in a lithography system for producing at least one electron beam (15) directed towards and focussed on an object (10) to be processed, said electron source (7) comprising at least one field emitter, characterized in that said electron source (7) comprises a semiconductor layer (16) with at least one tip (19), and said use includes the steps of:

- receiving light by said semiconductor layer (16);
- exciting electrons to a conduction band (E_c) by said light within said semiconductor layer (16) by a photo-electric effect;
- accelerating said electrons in said conduction band (E_c) towards said at least one tip (19) and tunnelling them outside said at least one tip (19) in order to generate electrons for said electron beam (15).

2. Use according to claim 1, wherein the lithography system comprises at least one microlens (2) to produce one light beamlet (12) directed to a mask (3) located in a mask location and an optical demagnifier (14) for demagnifying said light beamlet (12) by a predetermined factor and focusing the beamlet (12) on said electron source (7)

3. Use according to claim 1 or 2, wherein said semiconductor layer comprises silicon.

4. Use according to claim 3, wherein said silicon is p-doped.

5. Use according to any of the claims 1-4, wherein said at least one tip has a front surface with a diameter of 100 nm or less.

6. Use according to claim 5, wherein said diameter is 50 nm or less.

7. Use according to any of the preceding claims, wherein said semiconductor layer (16) comprises a plurality of tips (19).

8. Use according to claim 7, wherein said plurality of tips have intermediate spaces

of less than 8 μm.

9. Use according to claim 7 or 8, wherein said plurality of tips have heights of 8 μm or less.

10. Use according to any of the preceding claims, wherein said electron beam (15) is generated by an electric field and focussed by a magnetic field.

11. A lithography system comprising an electron source (7) for receiving light and converting said light in at least one electron beam (15) directed towards and focussed on an object (10) to be processed, said electron source (7) comprising at least one field emitter, characterized in that said electron source (7) comprises a semiconductor layer (16) with at least one tip (19), and said lithography system being arranged to:

- receive said light by said semiconductor layer (16);
- excite electrons to a conduction band (E_c) by said light within said semiconductor layer (16) by a photo-electric effect;
- accelerate said electrons in said conduction band (E_c) towards said at least one tip (19) and tunnel them outside said at least one tip (19) in order to generate electrons for said electron beam (15).

12. Lithography system according to claim 11, wherein said system comprises at least one microlens (2) to produce one light beamlet (12) directed to a mask (3) located in a mask location and an optical demagnifier (14) for demagnifying said light beamlet (12) by a predetermined factor and focusing the beamlet (12) on said electron source (7).

13. Lithography system according to claim 11 or 12, wherein said semiconductor layer comprises silicon.

14. Lithography system according to any of the claims 11-14, wherein said at least one tip has a front surface with a diameter of 100 nm or less.

16. Lithography system according to claim 15, wherein said diameter is 50 nm or less.

17. Lithography system according to any of the claims 11-16, wherein said semiconductor layer (16) comprises a plurality of tips (19).

18. Lithography system according to claim 17, wherein said plurality of tips have intermediate spaces of less than 8 μm.

19. Lithography system according to claim 17 or 19, wherein said plurality of tips have heights of 8 μm or less.

20. Lithography system according to any of the claims 11-19, wherein said electron beam (15) is generated by a magnetic and an electric field.

21. Lithography system according to claim 12, wherein said system comprises a plurality of microlenses (2) to produce a plurality of light beamlets (12).

22. Lithography system according to claim 21, wherein said system comprises between 10^6 and 10^8 microlenses (2).

23. Lithography system according to any of the claims 11-22, wherein said semiconductor layer (7) has a thickness of less than 30 μm, preferably less than 100 nm.

24. Lithography system according to any of the claims 11-23, wherein the semiconductor layer (16) is provided with at least one hole (20) surrounding said at least one tips (19).

Fig 1

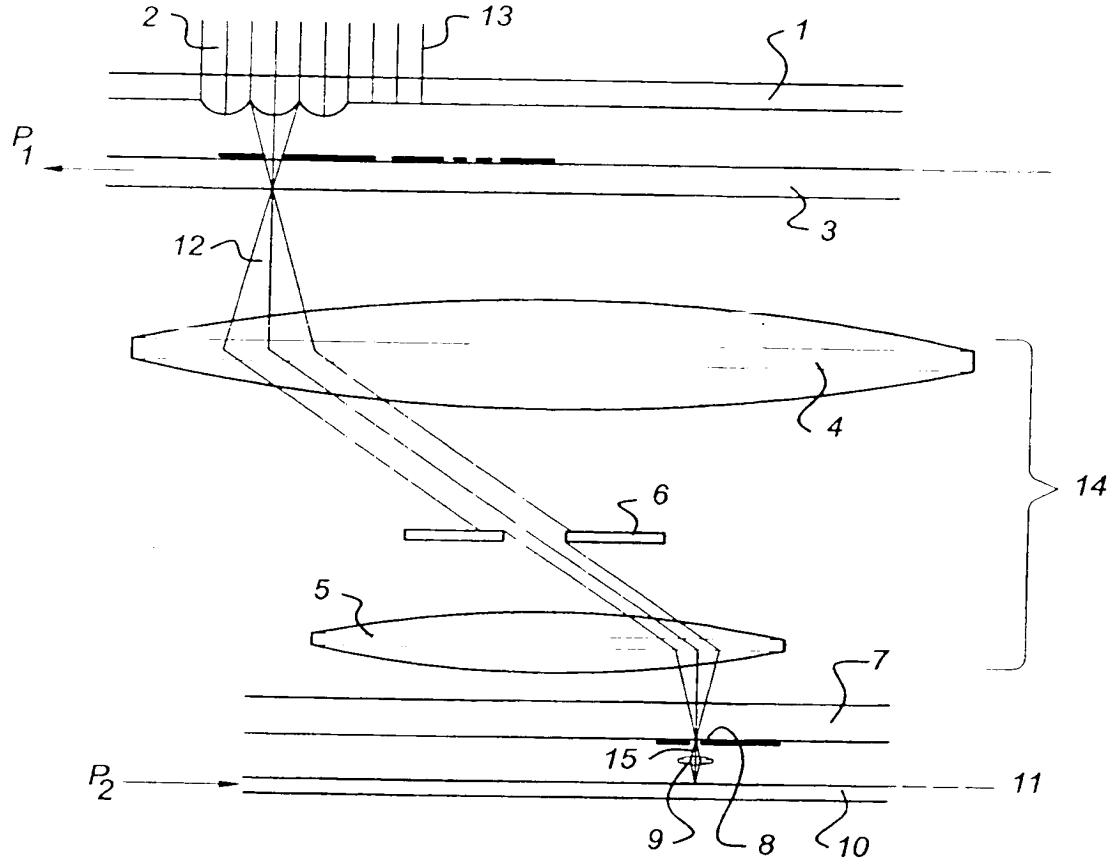


Fig 2

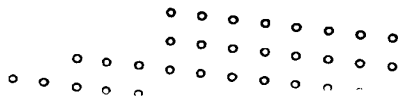


Fig 3

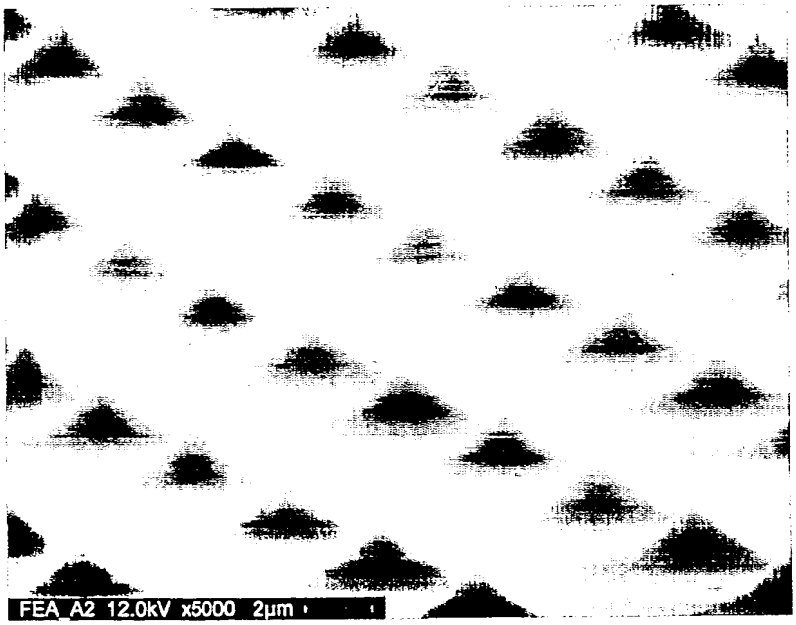

FEA A2 12.0kV x5000 2µm

Fig 4

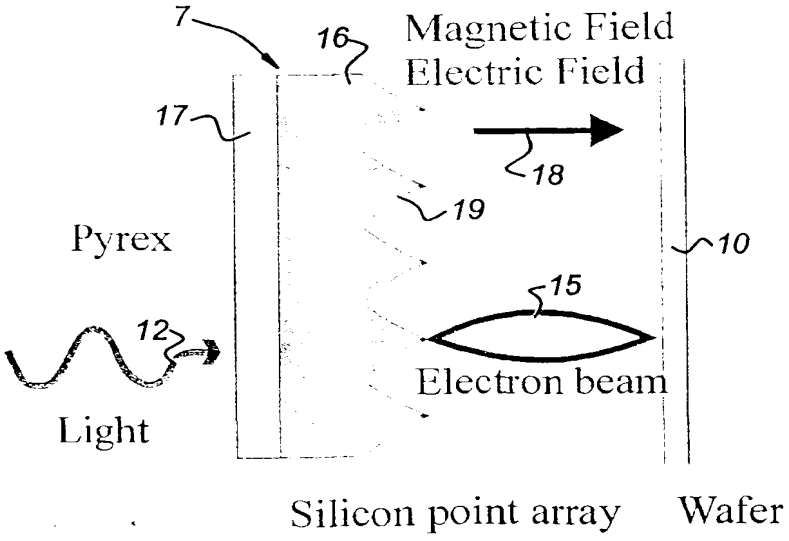

7
16
Magnetic Field
Electric Field
17
18
19
Pyrex
10
15
12
Electron beam
Light
Silicon point array
Wafer

Fig 5

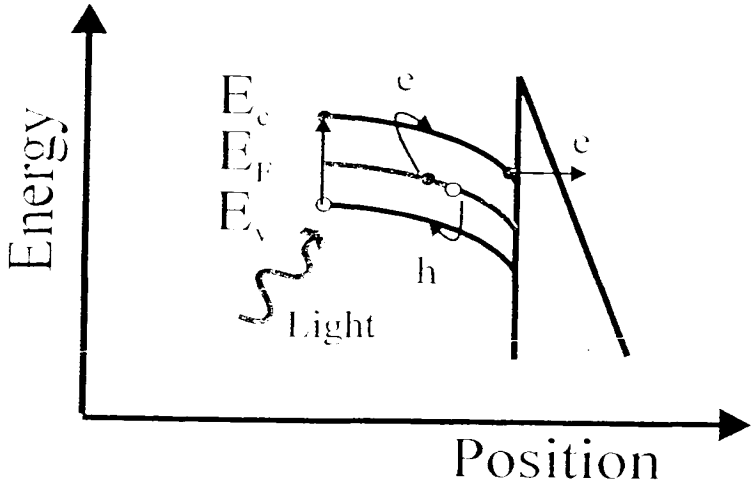


Fig 6

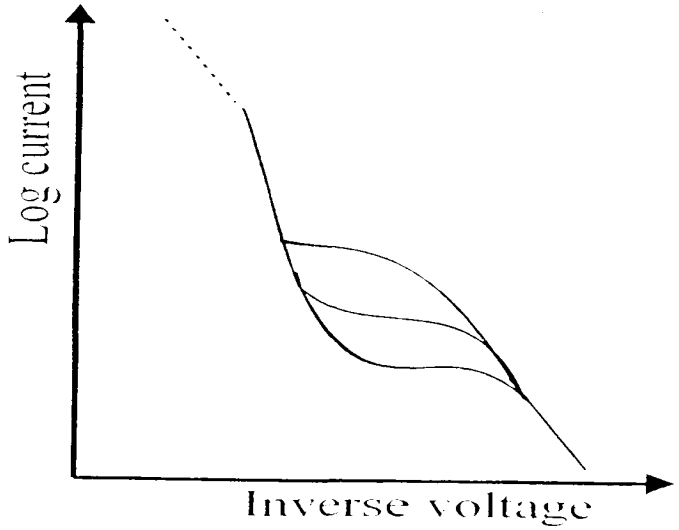


Fig 7

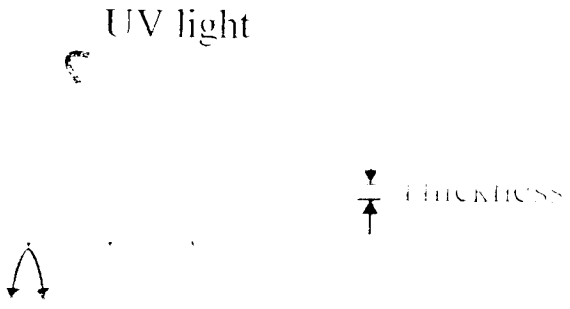


Fig 8a

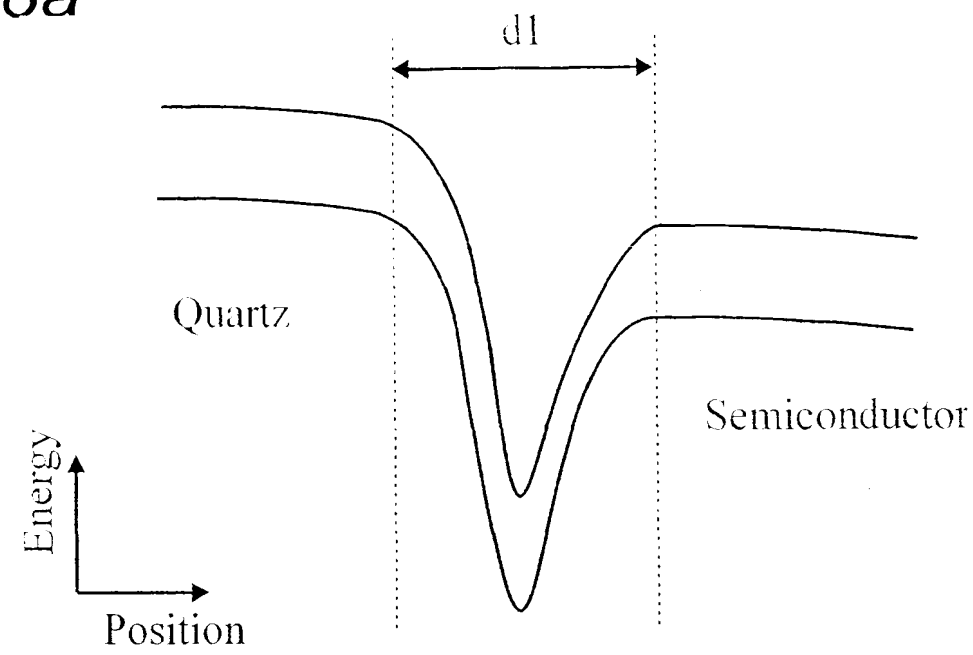

d1
Quartz
Semiconductor
Energy
Position

Fig 8b

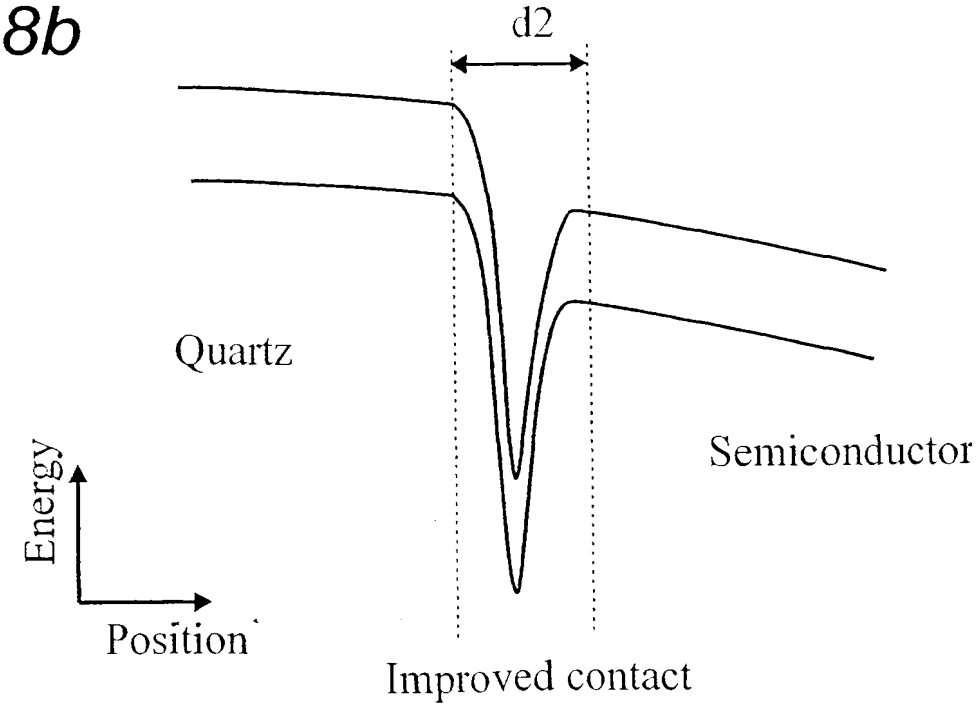

d2
Quartz
Semiconductor
Energy
Position
Improved contact

Fig 9a

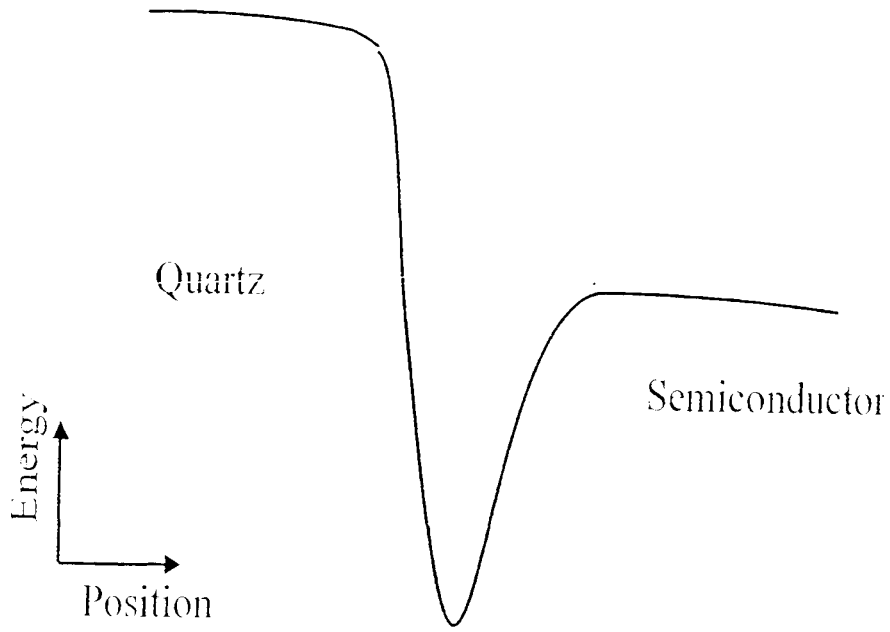

Quartz
Semiconductor
Energy
Position

Fig 9b

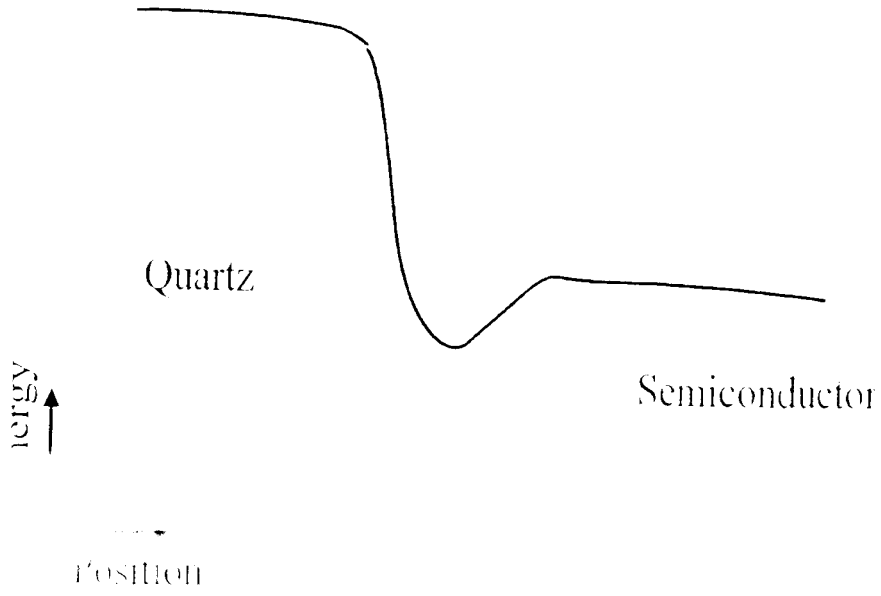

Quartz
Semiconductor
ergy
Position

Fig 10a

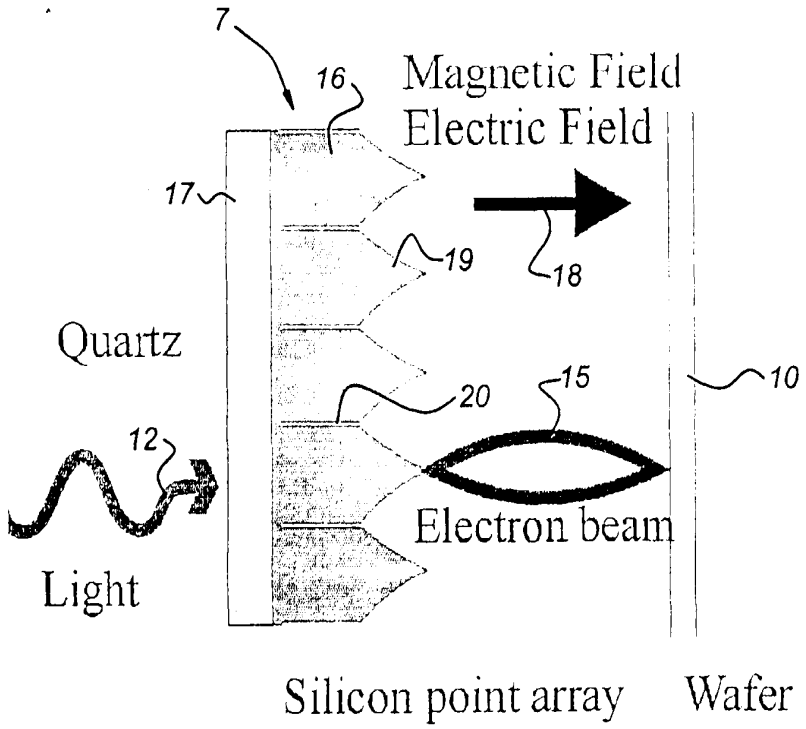
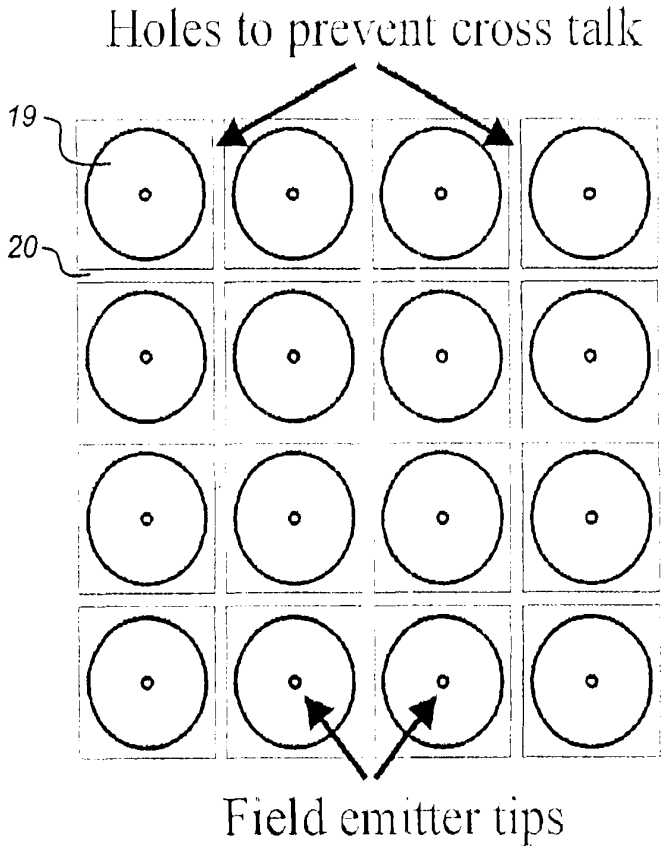


Fig 10b



INTERNATIONAL SEARCH REPORT

International Application No
PCT/NL 00/00657

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01J37/073 H01J1/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01J G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 881 542 A (TNO) 2 December 1998 (1998-12-02) cited in the application column 3, line 16 -column 4, line 50 column 6, line 22 - line 25 figures 1,5	1-4,7, 10-14, 17,20,21
Y	US 3 894 332 A (NATHANSON HARVEY C ET AL) 15 July 1975 (1975-07-15) column 1, line 56 -column 2, line 20 column 3, line 49 -column 4, line 14 figures 3,4,15	1-4,7, 10-14, 17,20,21
A	US 5 932 966 A (SCHNEIDER JAMES E ET AL) 3 August 1999 (1999-08-03) column 4, line 28 -column 5, line 35 figure 1	1,11

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/NL 00/00657

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SCHRODER D K ET AL: "THE SEMICONDUCTOR FIELD-EMISSION PHOTOCATHODE" IEEE TRANSACTIONS ON ELECTRON DEVICES. IEEE INC. NEW YORK, US, vol. 21, no. 12, December 1974 (1974-12), pages 785-798, XP000960813 ISSN: 0018-9383 cited in the application page 785, column 1, paragraph 2 - column 2, paragraph 1 figure 10	1,11

Form: PCT/ISA/210 (continuation of second sheet) (July 1992)

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